



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Sriram Satakopan et al.

Title: LOW THRESHOLD VOLTAGE TRANSISTOR DISPLACEMENT IN A SEMICONDUCTOR DEVICE

Application No.: 10/657,964

Filed: September 9, 2003

Examiner: Unknown

Group Art Unit: Unknown

Atty. Docket No.: 004-8841

November 6, 2003

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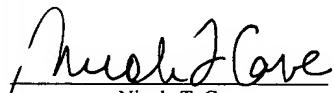
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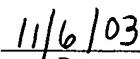
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Respectfully submitted,



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U.S. Department of Commerce, Patent and Trademark Office		Attorney Docket No.: 004-8841
		Application No.: 10/657,964
O INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>NOV 10 2003</i>		Applicant(s): Sriram Satakopan et al.
(Use several sheets if necessary)		Filing Date: September 9, 2003
		Group Art Unit: Unknown
		Date Submitted: November 6, 2003

U.S. Patent Documents				
*Examiner Initial		Document Number	Date	Name
	1	5,774,367	Jun. 30, 1998	Reyes et al.
	2	6,087,886	Jul. 11, 2000	Ko
	3	6,107,834	Aug. 22, 2000	Dai et al.
	4	6,396,749	May 28, 2002	Al-Shamma et al.
	5	US2002/0099989 A1	Jul. 25, 2002	Kawabe et al.
	6	US2002/0144223A1	Oct. 3, 2002	Usami et al.

Foreign Patent Documents					Translation	
		Document	Date	Country	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
	7 Elrabaa et al., "A Contention-Free Domino Logic for Scaled-Down CMOS Technologies with Ultra Low Threshold Voltages," IEEE International Symposium on Circuits and Systems, May 28-31, 2000, pages 1-748 through 1-751.
	8 Fujii et al., "A Sub-1V Dual-Threshold Domino Circuit Using Product-of-Sum Logic," International Symposium on Low Power Electronics and Design, August 2001, pages 259-262.
	9 Kao et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE Journal of Solid-State Circuits, Vol. 35, No. 7, July 2000, pages 1009-1018.
	12 McPherson et al., "760 MHz G6 S/390 Microprocessor Exploiting Multiple V_t and Copper Interconnects," IEEE, ISSCC, Feb. 7, 2000, pages 96-97.
	11 Miyake et al., "Design Methodology of High Performance Microprocessor using Ultra-Low Threshold Voltage CMOS," IEEE Custom Integrated Circuits Conference, May 6-9, 2001, pages 275-278.
	12 Mutoh et al., "A 1-V Multithreshold-Voltage CMOS Digital Signal Processor for Mobile Phone Application," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pages 1795-1802.
	13 Shibata et al., "A 1-V, 10-MHz, 3.5-mW, 1-Mb MTCMOS SRAM with Charge-Recycling Input/Output Buffers," IEEE Journal of Solid-State Circuits, Vol. 34, No. 6, June 1999, pages 866-877.
	14 Takamiya et al., "High Drive-Current Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body Effect and Low Threshold Voltage," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pages 1633-1640.
	15 Tripathi et al., "Optimal Assignment of High Threshold Voltage for Synthesizing Dual Threshold CMOS Circuits," IEEE, January 7, 2001, pages 227-232.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.